

## Appendix A: Supported Rabbit 3000 Baud Rates

This table contains divisors to put into TATxR registers. All frequencies that allow 57600 baud up to 30MHz are shown (as well as a few higher frequencies). All of the divisors listed here were calculated with the default equation given on the next page.

Crystal Freq. (MHz)	2400 baud	9600 baud	19200 baud	57600 baud	115200 baud	230400 baud	460800 baud
1.8432	23	5	2	0	a	-	-
3.6864	47	11	5	1	0	-	-
5.5296	71	17	8	2	-	-	-
7.3728	95	23	11	3	1	0	-
9.2160	119	29	14	4	-	-	-
11.0592	143	35	17	5	2	-	-
12.9024	167	41	20	6	-	-	-
14.7456	191	47	23	7	3	1	0
16.5888	215	53	26	8	-	-	-
18.4320	239	59	29	9	4	-	-
20.2752	b	65	32	10	-	-	-
22.1184	*	71	35	11	5	2	-
23.9616	*	77	38	12	-	-	-
25.8048	*	83	41	13	6	-	-
27.6480	*	89	44	14	-	-	-
29.4912	*	95	47	15	7	3	1
36.8640	*	119	59	19	9	4	-
44.2368	*	143	71	23	11	5	2
51.6096	*	167	83	27	13	6	-

- a. Baud rate is not available at given frequency.
- b. Baud rate is available with further BIOS modification.

The default equation for the divisor is:

$$\text{divisor} = \frac{\text{CPU frequency in Hz}}{32 \times \text{baud rate}} - 1$$

If the divisor is not an integer value, that baud rate is not available for that frequency (identified by a “-” in the table). If the divisor is above 255, that baud rate is not available without further BIOS modification (identified by a “\*” in the table). To allow that baud rate, you need to clock the desired serial port via timer A1 (by default they run off the peripheral clock / 2), then scale down timer A to make the serial port divisor fall below 256.

Timer A can be clocked by the peripheral clock (**PCLK**) in addition to the default, which is the peripheral clock/2 (**PCLK/2**). Furthermore, the asynchronous serial port data rate can be 8x the clock in addition to the default of 16x the clock. Therefore, in addition to the equation above, the following equations may be used to find the asynchronous divisor for a given clock frequency.

Timer A clocked by **PCLK/2**, serial data rate = 16 x clock

$$\text{divisor} = \frac{\text{CPU frequency in Hz}}{16 \times 2 \times \text{baud rate}} - 1$$

Timer A clocked by **PCLK**, serial data rate = 16 x clock:

$$\text{divisor} = \frac{\text{CPU frequency in Hz}}{16 \times \text{baud rate}} - 1$$

Timer A clocked by **PCLK/2**, serial data rate = 8 x clock:

$$\text{divisor} = \frac{\text{CPU frequency in Hz}}{8 \times 2 \times \text{baud rate}} - 1$$

Timer A clocked by **PCLK**, serial data rate = 8 x clock:

$$\text{divisor} = \frac{\text{CPU frequency in Hz}}{8 \times \text{baud rate}} - 1$$